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09/649,539	08/28/2000	Masato Tanaka	6715/62963	8465

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EXAMINER

WEST, JEFFREY R

ART UNIT

PAPER NUMBER

2857

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/649,539

Applicant(s)

TANAKA ET AL.

Examiner

Jeffrey R. West

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because its length exceeds the 150 word limit. Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities:

On page 17, line 4, the "polar conversion section" is incorrectly labeled "5" instead of "6", as it is labeled on page 10, line 19, and in Figure 3.

On page 44, line 1, the "comparator" is incorrectly labeled "7T" instead of "75", as it is labeled on page 44, line 15, and in Figure 25.

On page 54, line 17, it is unclear why the applicant refers to "multiplier 82" as both the third and second multiplier.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 3, and 16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 1 and 16 are rejected under 35 U.S.C. 112, first paragraph, because in the background of the invention, the applicant explains that, "when the low pass filter is directly applied to the angle signal, filtering cannot be preformed precisely". Since claims 1 and 16 recite an apparatus comprising "a low pass filter for removing a high pass component in said angle signal output from said polar conversion section", they claim the incorrect process that the invention is trying to overcome. This discrepancy makes the invention of claims 1 and 16 unclear.

Claim 3 is rejected under 35 U.S.C. 112, first paragraph, because it recites a low pass filter comprising a "second increase and decrease means for increasing or decreasing said phase error output from said first increase and decrease means". The description of the low pass filter on page 29, lines 1-5, and the corresponding block diagram, Figure 20, do not describe any means for selectively increasing or decreasing a signal, as suggested in claim 3, only increasing means (i.e. adders) and a phase comparator that comprises a subtraction circuit. Further, claim 3, describes a first increase and decrease means for increasing or decreasing the phase error output from the phase comparator, while Figure 20, and the description on page 29, lines 14-18, provide a guard circuit (37) and amplifier (32) receiving the phase error output from the phase comparator (31). Figure 20 also shows the phase error integrator (34), comprising an adder, receiving a signal from a second amplifier (33), not an increase and decrease means, as claimed. Because, in claim 3, as well as in the specification, there is no distinction between adders that are internal to another component and adders that are separate components, no indication of a

means for selectively increasing or decreasing a signal, and no mention of using two increasing or decreasing means sequentially, as is suggested by the claim, it is unclear how to implement the invention of claim 3.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-18 are rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite.

Claim 1 is rejected as being vague and indefinite because the limitation "a recording medium on which a position signal having a periodic signal is recorded" is unclear. It is suggested that this limitation be rewritten as ---a recording medium on which a periodic position signal is recorded---. It is also unclear, in claim 1, what is intended in the limitation "an angle signal representing a relative position of said recording medium and said detection in one period as an angle".

Claims 2 and 17 are considered vague and indefinite because they recite "wherein said frequency control oscillator controls said frequency of said periodic signal such that said phase error is zero based on said frequency control signal, and outputs said periodic signal as said angle signal from which said high pass component has been removed". It is unclear what it means to output "said periodic signal as said angle signal", since the angle signal is already defined as the output of a polar conversion section, in claim 1. This lack of clarity is also present in claims 4 and 5 that recite, "said angle signal output from said frequency control oscillator"

because the angle signal has already been designated as the output of the polar conversion section.

Claim 4 is further rejected as being vague and indefinite because it specifies "an adder" that is different than "an adder" specified in parent claim 2.

Claim 3 is rejected as being vague and indefinite because it includes the limitation "wherein said integrator integrates said phase error increased or decreased by said second increase and decrease means". This limitation is inconsistent with the limitation of parent claim 2, which recites "an integrator for integrating said phase error output from said phase comparator". Since claim 2 describes integrating the output of the phase comparator, and claim 3 describes integrating the output of the second increase and decrease means, using the same integrator, claim 3 is unclear. Claim 3 is also considered vague and indefinite because of the limitation "said phase error output from said increase and decrease means" since claim 3 recites two separate increase and decrease means, and this limitation fails to specify which one is being designated.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite because it includes the limitation of a "third increase and decrease means", when there is no mention of any first or second increase and decrease means in the parent claims. Claim 5 is also vague because it recites "said adder" without specifying whether it is referring to the adder of the prediction section, in claim 4, that adds the velocity error output from the integrator and the angle signal output from the frequency control oscillator, or the adder from the low pass filter, in

claim 2, that adds the velocity error output from the integrator and the phase error output from the phase comparator.

Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite because it recites "an angle signal showing an angle in one period". It is unclear what this limitation is trying to provide.

Claims 6-15 are rejected under 35 U.S.C. 112, second paragraph, as being vague and indefinite because they incorporate the faulty language present in their respective parent claims.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 2, 6, 8, 9, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,140,245 to Stacey in view of U.S. Patent No. 5,734,172 to Pryor et al. and U.S. Patent No. 5,432,443 to Maejima et al.

Stacey discloses a position detection apparatus for generating a signal representing the absolute angular position of a rotating shaft (column 3, lines 4-6) comprising three operational integrators that obtain voltage signals representing phase (column 3, lines 17-25), a phase locked loop containing phase comparators,

in the form of multiplying digital to analog converters, which receive the phase signal from the operational integrators to generate a phase error signal (column 3, lines 39-54), and a means for generating a total phase error signal using an adder that sums the values of the individual phase errors, and an error integrator, that integrates the phase error signal to obtain a speed/velocity error signal (column 4, lines 4-7). Stacey also includes an absolute value circuit that applies the phase error signal, functioning as a frequency control signal, to a frequency controlled oscillator that generates a periodic pulse signal having a variable frequency proportional to the phase error signal (column 3, lines 54-59), and a low pass filter that filters the high pass component from the received signal magnitude and outputs the filtered signal to a comparator for indicating the presence the phase error (column 4, lines 14-19).

Stacey also discloses operation of the phase locked to keep the size of the phase error, output by the multiplying digital to analog converters (as noted above, functioning as a phase comparator), exactly zero. To keep this phase error zero, Stacey describes temporarily increasing or decreasing the frequency (i.e. adjusting the gain, since the gain of the phase integrator is inversely proportional to the frequency (column 3, lines 20-21)) of the of the frequency controlled oscillator, to control the outputted periodic pulse signal, using an absolute value circuit that determines the absolute value of the phase error output by the phase comparator (column 4, lines 65-68). Stacey also discloses outputting an angular position of the device being tested (column 3, lines 5-6 and 39-41).

With respect to claims 12 and 13, although Stacey does not specifically disclose adjusting the gain of the signal when the absolute value of the phase error exceeds a predetermined level, it is inherent that in order for the absolute value circuit to decrease the gain/frequency of the frequency controlled oscillator when the phase error output by the summing junction becomes positive (column 5, lines 5-12), that the absolute value circuit must have the value of zero set as a predetermined threshold and adjust the gain when the predetermined threshold is exceeded (i.e. the error becomes positive) for some period of time.

As noted above, the invention of Stacey does include obtaining signals from the device in both magnitude and phase form, but does not specifically describe converting the position signal into polar coordinates, angle and amplitude, or specify that the detection section comprise two detection heads, spaced apart, that move along a recording medium to read a periodic position signal.

Pryor teaches a method and apparatus for determining the dimension, location, and attitude of objects comprising two sensors located on opposite sides of a detection head (column 10, line 66 to column 11, line 6) wherein measurements taken by the sensors, to determine the parameters of a mechanical system that specifically require lead deviation (i.e. amplitude) and angular direction information, can be measured in, or equivalently converted into, polar coordinates (column 7, lines 46-59)

It would have been obvious to one having ordinary skill in the art to modify the invention of Stacey to include converting the position signal into polar coordinates,

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as taught by Pryor, because, as suggested by Pryor, the combination would have provided accurate, fast, and smooth measurements when the detector of the invention is measuring position information of a concave surface (column 4, lines 49-57).

Maejima teaches a linear position detector comprising a scale (i.e. a recording medium) that contains a periodic position signal (column 3, lines 54-62 and Figure 3A) read by a pair of detecting heads to detect the longitudinal movement of the scale with respect to each head (column 3, lines 21-24), wherein the second detection head receives a separate signal from the first signal (column 4, lines 10-19) and is spaced apart by a predetermined distance to maintain a phase difference (column 3, lines 43-46). Further, since the detecting heads read a specific periodic signal from the recording medium, it is inherent that the detecting heads travel in the recording direction of the medium.

It would have been obvious to one having ordinary skill in the art to modify the invention of Stacey to include specifying that the detection section comprise two detection heads, spaced apart, that move along a recording medium to read a periodic position signal, as taught by Maejima, because, as suggested by Maejima, the combination would have provided the placement of the two detecting heads, specifically $(m + \frac{1}{4})\lambda$ apart where λ is a recording wavelength of the scale, so as to obtain two separate signals that provide the necessary phase difference needed to calculate the displacement of the scale (column 2, lines 14-20).

9. Claims 7, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stacey in view of Pryor and Maejima, and further in view of U.S. Patent No. 5,526,332 to Yamada et al.

As noted above, Stacey in combination with Pryor and Maejima teach all the features of the claimed invention, except for including a noise detection section for detecting internal noise of the received amplitude signal.

Yamada teaches a method for generating a reference clock used in optical disc servo control and for detecting positional deviation of the optical device (column 10, lines 53-55) comprising a device that produces a current signal, representing a recorded signal, by reading marks formed on a disc (column 7, lines 15-20).

Yamada teaches passing the representative current signal to a peak/amplitude detecting circuit (column 7, lines 20-25) wherein the amplitude signal is then sent to a noise detecting circuit (column 16, lines 1-3) to determine internal noise errors in the amplitude signal. Yamada then teaches stopping the output of the phase comparator, which determines the phase error of the frequency controlled PLL circuit (column 16, lines 28-36 and column 13, lines 22-41), if an error occurs in the amplitude signal.

It would have been obvious to one having ordinary skill in the art to modify the invention of Stacey, Pryor, and Maejima to include a noise detection section for detecting internal noise of the received amplitude signal, as taught by Yamada, because, as suggested by Yamada, the combination would have provided a method

for increasing the accuracy of phase error detection by preventing influence of internal noise on the PLL circuit (column 16, lines 37-40 and column 4, lines 3-13).

10. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stacey in view of Pryor and Maejima, and further in view of U.S. Patent No. 5,852,413 to Bacchi et al.

As noted above, Stacey in combination with Pryor and Maejima teach all of the features of the claimed invention, except for designating the received position signal as an address, and using a table to look-up the corresponding gray-coded angle.

Bacchi teaches an improved position encoding apparatus that conveys, positions, and orients a semiconductor wafer (column 3, lines 1-4) by converting detected position signals to angular data, using a look-up table that lists the angles and corresponding signal addresses (column 8, lines 19-36), before conveying the angular position information to an angular position register (column 6, lines 34-47). Bacchi also teaches using gray-coded data for the look-up table in a device that is operable to store the gray code encoders using more than three bits of data (column 2, lines 30-34).

It would have been obvious to one having ordinary skill in the art to modify the invention of Stacey, Pryor, and Maejima to include designating the received position signal as an address, and using a table to look-up the corresponding gray-coded angle, as taught by Bacchi, because, as suggested by Bacchi, the combination would have provided a rapid, high resolution (column 2, lines 33-34), and highly

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accurate (column 6, lines 48-63) method of determining the angular positions of the device.

11. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stacey, in view of Pryor and Maejima, and further in view of the applicant's admitted prior art.

As noted above, the invention of Stacey, Pryor, and Maejima teach all the features of the claimed invention except for specifying that the processing functions of the invention be included in an arithmetic processing unit.

In the background of the invention, the applicant admits as prior art, a well known position detecting apparatus for detecting a position of movement of two members which move relative to each other, comprising a scale on which a periodic signal is recorded, a head section for detecting the periodic signal recorded on the scale, and an arithmetic processing section for performing signal processing of the periodic signal, to output position information (page 1, lines 9-15). The applicant also admits as prior art that the arithmetic processing section processing of the well known position detecting apparatus include a polar conversion section to form an angle signal, and low pass filtering section (page 2, lines 3-5, 8-10, and 11-13).

It would have been obvious to one having ordinary skill in the art to modify the invention of Stacey, Pryor, and Maejima to include specifying that the processing functions of the invention be included in an arithmetic processing unit, as taught by the applicant's admitted prior art, because it would have provided a packaged

processing device needed for performing the functions of the position detecting apparatus.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,995,465 to Hayashi et al. teaches a digital signal reproducing apparatus comprising a voltage-controlled oscillator, low pass filter, phase control circuit, and a position detecting circuit.

U.S. Patent No. 5,668,331 to Schintag et al. teaches a position sensor comprising a phase comparator and low pass filter.

U.S. Patent No. 5,917,783 to Kobayashi et al. teaches a recording/reproducing apparatus and method for an optical disc using gray coded addresses comprising a detecting optical head, voltage-controlled oscillator, low pass filter, and phase comparator.

U.S. Patent No. 5,404,349 to Nose et al. teaches a position displacement detecting apparatus comprising a phase detector, oscillator, and low pass filters.

U.S. Patent No. 5,761,165 to Takeda et al. teaches a head radial position detecting circuit comprising a phase difference table and a PLL circuit.

13. Any inquiry concerning this communication or earlier communications from the

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examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday thru Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
April 22, 2002


MARC S. HOFF
SUPERVISORY PATENT EXAMINER
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